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B. E. (Seventh Semester) Examination, April-May 2020/NOV-DEC 2020

(New Scheme)

(Et & T Engg. Branch)

DIGITAL CIRCUIT DESIGN with VERILOG HDL

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Part (a) of each question is compulsory. Attempt any* ***two*** *parts from (b), (c) and (d) of each question.*

Unit-I

1. (a) Define complier directives in Verilog HDL. 2

(b) Differentiate system TASK and FUNCTIONS of Verilog HDL with an examples. 7

(c) Explain typical design flow of HDL withs its popularity in designing and Verification. 7

(d) Enlist data type used in Verilog HDL with its syntax. 7

Unit-II

2. (a) Enlist operator in Verilog HDL. 2

(b) Explain the gate level and stricter level modelling in Verilog. 7

(c) Design and implement a 4_bit Ripple adder using Structural modelling (using Full adder) Verilog HDL. 7

(d) Design and implement 16 : 1 Multiplexer using Generate block of 4 : 1 MUX in Verilog HDL. 7

Unit-III

3. (a) Differentiate Verilog and VHDL. 2

(b) Write the verilog code for a 3 : 8 decoder circuit. 7

(c) Draw the structure of 16 : 1 De-multiplexer and write down Verilog code. 7

(d) Write the verilog code for Binary to gray Code Converter. 7

Unit-IV

4. (a) What is Flip Flop? 2

(b) Write a verilog code for the BCD Counter. 7

(c) Design a T and J-K flip flop circuit Verilog HDL. 7

(d) Write a verilog code to design shift registers using 2 : 1 multiplexer only. 7

Unit-V

5. (a) Discuss More and Mealy FSM network. 2

(b) Write verilog HDL code of serial binary adder as a Mealy network. 7

(c) Design and implement Vending Machine. 7

(d) Explain the relevance of implication table in state machine concepts. 7